AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 4, line 7, with the following amended paragraph:

FIG. 1 is a schematic functional block diagram showing an exemplary arrangement of an imager 1 that effectively supports interlace scan (IS) operation, dynamic range widening scan (WS) operation and sequential scan (SS) operation in accordance with an illustrative embodiment of the invention. In FIG. 1, the imager 1 comprises an optical and mechanical portion (OMP) 10 for focusing into an image of the object to be shot; an OMP driver 12 for driving the optical and mechanical portion 10 in responsive to control signals supplied from the external; a CCD (charge coupled device) portion 14 that operates in one of three (i.e., IS, WS and SS) operation modes in response to a IS/WS/SS selection signal supplied from the outside of the imager 1 (i.e., from a not-shown controller for controlling the entire video camera in which the imager 1 is used); a preprocessor ~~116~~ (not shown) for effecting analog processing (e.g., AGC (automatic gain control)) of the image signal from the CCD portion 14; an analog-to-digital converter (A/C) ~~18~~ 16 for converting the analog image signal from the preprocessor 16 into a digital image signal; a synchronizer 30 for providing a time axis conversion in the dynamic range widening scan (WS) operation or in the sequential scan operation; a signal mixer 40 for mixing two image signals of different exposure (or charging) times into a dynamic range-widened image signal in the WS operation mode; an image signal regulator 50 for providing basic camera signal processing such as contour correction; a sequentially scanned image signal generator 60 for composing a single sequential scan image signal from an odd line field signal and an even line field signal into which a sequential scan image signal has been separated by the time axis conversion 30 in the SS mode; an IS and WS signal output portion 70 for outputting an IS or WS

image signal depending on the operation mode; and an imager controller 80 for supplying various control signals to respective elements as detailed later.

Please replace the paragraph beginning at page 5, line 19, with the following amended paragraph:

The signal mixer 40 comprises a ~~mixer 42~~ mix and gradation correction 42 having its one data input 42L connected to the selector 36 common terminal, its the other data input 42S connected to a second one (34-2 in this specific example) of two 1H-memories 34 and its control input connected to a control output WS of the imager controller 80; and a third alternative selector 44 having one data input 44A connected to the selector 36 common terminal and the mixer input 42L, the other data input 44B connected to the mixer 42 output and a selector 32 input 32B and its control input terminal connected to the control output WS of the imager controller 80. The control signal WS takes a binary value depending on whether the operation mode of the imager 1 (or the CCD portion 14) is in the dynamic range widening scan (WS) mode or not. It is assumed that the signal WS is logical "1" in case of the WS mode. Then, the mixer 42 is so arranged as to add the L input signal, which has been longer exposed or charged, and the S input signal, which has been shorter exposed or charged, yielding a dynamic range-widened image signal and to effect an gradation correction on the dynamic range-widened image signal if the imager 1 is in the WS mode. Though the common terminal of the alternative selector 36 is supplied to the A input of selector 44 in the interlace scan (IS) mode and the sequential scan (SS) mode, the selector 36 common terminal may be gradation corrected in the mixer 42 and then supplied to the B input of the selector 44 in the IS and SS modes.

Please replace the paragraph beginning at page 6, line 21, with the following amended paragraph:

The IS and WS (or Sm) signal output portion 70 comprises an adder 72 that is utilized in the SS mode for adding the first and second outputs of the image signal regulator 50, which are an odd line signal and an even line signal in the mode, to generate an interlace scanned image signal; and a ~~third~~ fourth alternative selector 74. The image signal regulator 50 first output is connected to an (odd) input of the SS image signal generator 60, the adder 72 first input and a first input of the adder 72 and a selector input 74B. The image signal regulator 50 second output is connected to an (even) input of the SS image signal generator 60 and the adder 72 second input. The selector 74 has its control input connected to the SS control output of the imager controller 80. The SS control signal takes a binary value depending on whether the imager 1 or the CCD portion 14 is in the SS mode or not. The selector 74 and the controller 80 (or the control signal SS) is so configured as to output the selector 74A input signal in the SS mode and to output the selector 74B input signal in other scan or operation mode.